Trigger Circuit for Fast Response Photodiode

Supervised Learning Project
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Abstract

Scintillation detectors are used in many nuclear physics and particle physics experiments because of many attractive properties like their linear response to energy and fast response times. The light output of scintillators needs to be amplified for readout. Photomultiplier tubes are most commonly used for this purpose, but they are bulky and require very high operating voltages. In this project, a simple transimpedance amplifier with a fast photodiode is used to replace the bulky photomultiplier tube. Basic building blocks would be a pre-amplifier, a trigger circuit and a pulse shaping module. The pre-amplifier will make the signal from the photodiode big enough for analysis and when we get a signal the trigger circuit triggers and set t=0, thus reading in the data, shaping, and then storing it for analysis. The trigger circuit helps to keep the required data and discard the unwanted the data, thus giving us a better runtime.

Certificate of Merit

This is to certify that **Mr. Harsh Kabra** has done a course project on experimental particle physics by building a **Triggering Module**.

Prof. Pradeep Sarin

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Remarks:

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Contents

Chapter 1

Trigger

1.1 What is a trigger?

In experimental particle physics, the experiments are generally in search of specific reactions that happen, which may have a less branching ratio/single event sensitivity. Thus a lot of other reactions occur which also send some signals to the measuring instruments. This creates a lot of events to be recorded. Out of these only a selected few are actually of interest. Storing all the events in memory is undesirable as many events are not useful for research and consume a lot of space. In order to overcome these drawbacks a trigger is used which will decide when to store the data and when to ignore the signal.

A trigger is basically an `"if..else"` statement being executed during the experiment in the electrical circuit.

1.2 Trigger system for photo diode

The general signal rate is 10 Hz to 100 Hz but the signals have rise time of order of micro seconds thus we definitely need a trigger system to eliminate the background events and noise coming from the surrounding.

1.3 Discriminators

The discriminator is a device which responds only to input signals with a pulse height greater than a certain threshold value. If this is satisfied, the discriminator responds by creating a logic signal; if not, no response is made. The value of the threshold can usually be adjusted. As well, an adjustment of the width of the logic signal is usually possible via similar controls. The most common use of the discriminator is for blocking out low amplitude noise pulses from photo multipliers or other detectors. Good pulses, which should in principle be large enough to trigger the discriminator, are then transformed into logic pulses for further processing by the following electronics. This trigger sends a signal to the DAQ to start taking the reading and storing it for future reference.

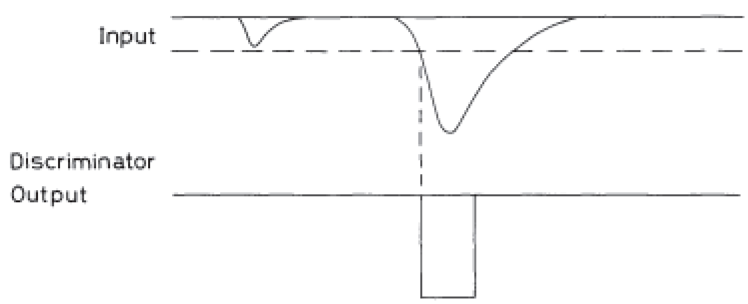


Figure 1.1: Functioning of a discriminator

1.4 Constant Fraction Discriminator

A Constant Fraction Discriminator is the one of the best methods of triggering a signal, where we know that the rise time of all the signals will be the same.

So if we keep a basic discriminator as our sole trigger system, there might be a few problems like data loss as well as two simultaneous signals in real time will be triggered at different times by the DAQ.

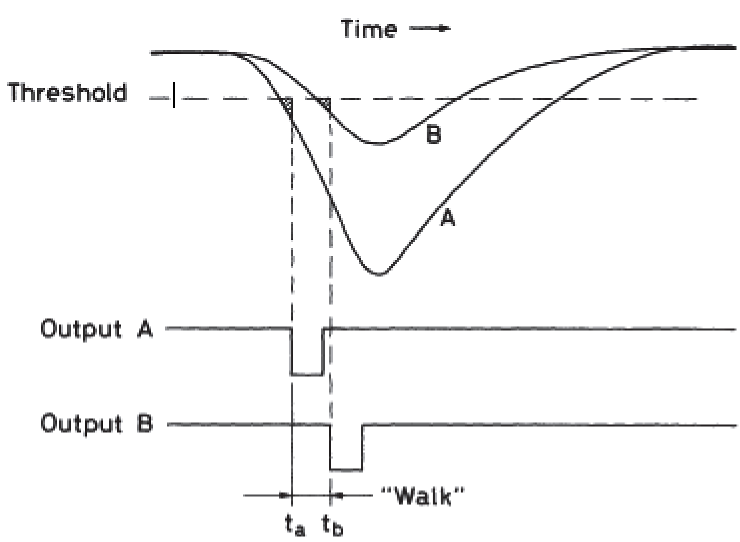


Figure 1.2: The drawback of just using a simple discriminator

As you can see that for the signal having same rise time but different amplitudes are triggered at different times. Thus leading the DAQ to start late and hence losing on the data which is of interest.

This is where Constant Fraction Discriminator comes in.

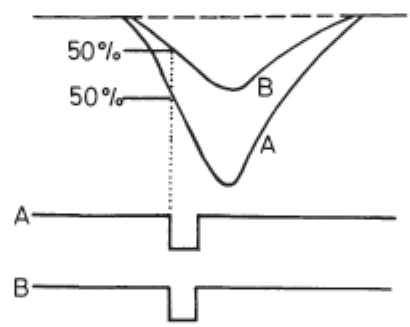


Figure 1.3: The ideal CFD working

We need something like this to happen and CFD exactly does what is shown.
For this to happen we need to split the signal into 2 parallel signals out of which one is inverted and attenuated by a factor f and the other is delayed by a time τ.

$$\tau = t_{delay} = f * t_{rise}$$

Where f is the fraction at which the circuit must be triggered. Due to this delay the attenuated signals peak height coincides with the the delayed signal at a value which is that fraction f of the original peak height, thus leading to a zero crossing at that point. The circuit gets triggered at the zero crossing.

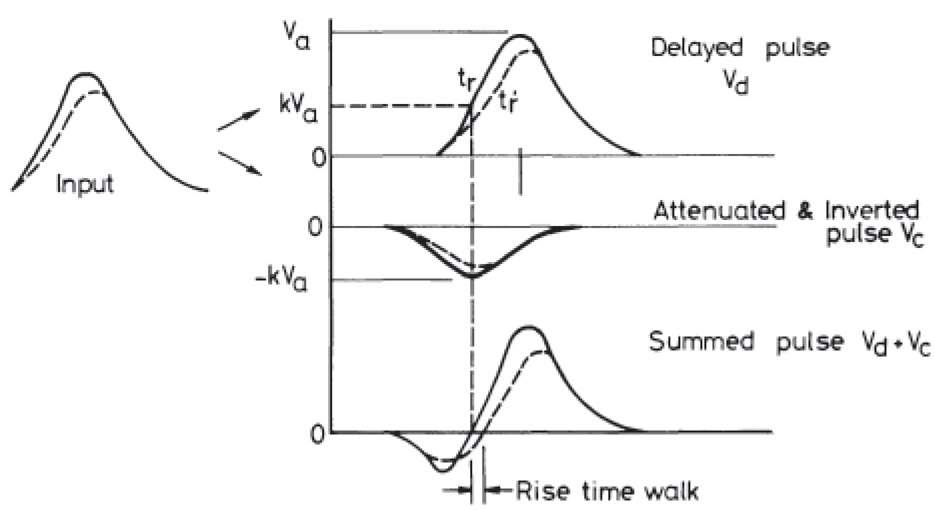


Figure 1.4: The drawback while creating a CFD module, i.e. the rise time walk.

But the main drawback of CFD is that the signals must have same rise time, only then the CFD will work at maximum efficiency.
So if we have signals of different rise time, there will be a rise time walk, which we dont want.

As one can see the the figure above that, two simultaneous signals with different rise time get their zero crossings at different time, because of this rise time walk, the circuit will be triggered at a different time. This will pose a problem to the Data Acquisition System(DAQ) as, the measurement of the peak height of the pulse will not be the actual peak height. Thus in search of a new method that, will eliminate the rise time walk, so that the DAQ is as accurate as possible, technically.

1.5 Amplitude and Rise time Compensation

This method of triggering is used for signals whose rise time as well as amplitudes are uncertain. It is almost same as constant fraction discriminator (CFD) but the difference is about the delay of the signal which is added to get zero triggering is less the the fraction of rise time that is used in CFD.

$$t_{delay} < f * t_{rise}$$

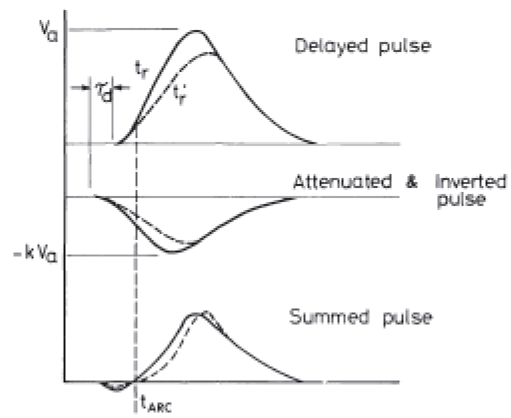


Figure 1.5: The best method which can give no rise time walk defects

This method ensures the zero crossing to be the same, for all signals irrespective of amplitude and rise time. Thus the trigger system will be quite efficient and certain.

Challenges to be implemented

Creating a tunable Analog Delay Circuit

In order to get the zero crossing at the appropriate point, there must be a really accurate tunable delay module.

Fast response circuit

As the signal might of a few millivolts, so the circuit needs to respond to that.

Unfortunately these challenges are more dependent on device fabrication as they demand accuracy rather than logic. Since we dont know the specific rise time for the signal, we cant possibly create an accurate delay circuit.
The ARC method requires

$$t_{delay} < f * t_{rise}$$

Taking $t_{delay} \approx 10^{-9}s$ which can be simply achieved by simply sending the signal to the adding circuit without any affect on it.

Basically this is like implementing a Schmidt Trigger Circuit with the threshold voltage 100mV.

1.6 Simulation

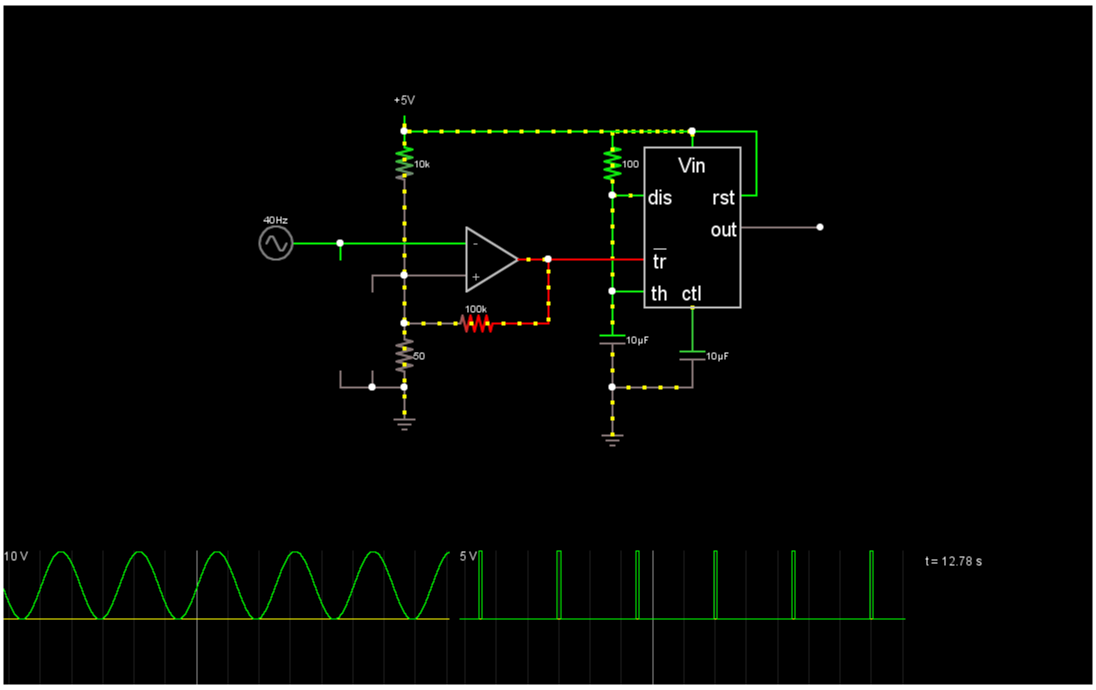


Figure 1.6: A simulation of working of a basic Schmidt Trigger circuit

As can be seen in the figure that an inverting schmidt trigger circuit is used in order to use the IC 555 timer in monostable mode as its output goes high when the trigger pin 2 goes below one third V_{cc}, thus inverting first half.
The left graph is the input signal and the graph on the right shows the output from the timer which is a pulse of amplitude 5 V and pulse width 1ms which can be tuned by to send an indication to the DAQ for setting its t=0 and starting data acquisition after time $t = t_{rise}$. Thus the circuit is working as per requirement.

Lets build it!

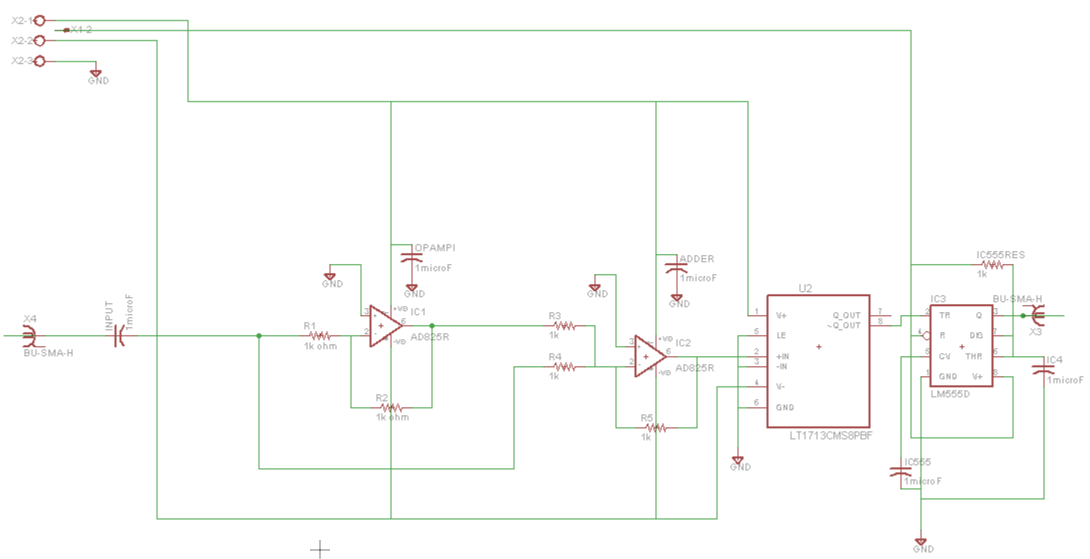
Chapter 2

Building the circuitry

Working on the Amplitude and Rise time Compensation (ARC) triggering circuit, the most effective, in which the input was a signal from the pre-amplifier and my circuit has to send a pulse at the time of triggering to the data acquisition system(DAQ). Putting together a few high speed opamps, comparator and an IC 555 timer to send a pulse to the DAQ, along with some resistors the circuit was ready to be made.

EAGLE software was used to make the circuit and create the board to be fabricated at the PCB lab at IIT Bombay by the chemical etching method.

2.1 Schematic



As can be seen in the schematic, the input signal is split into two separate line. In one line there is an Inverting Opamp with gain set less than 1 i.e. the gain is the fraction f.

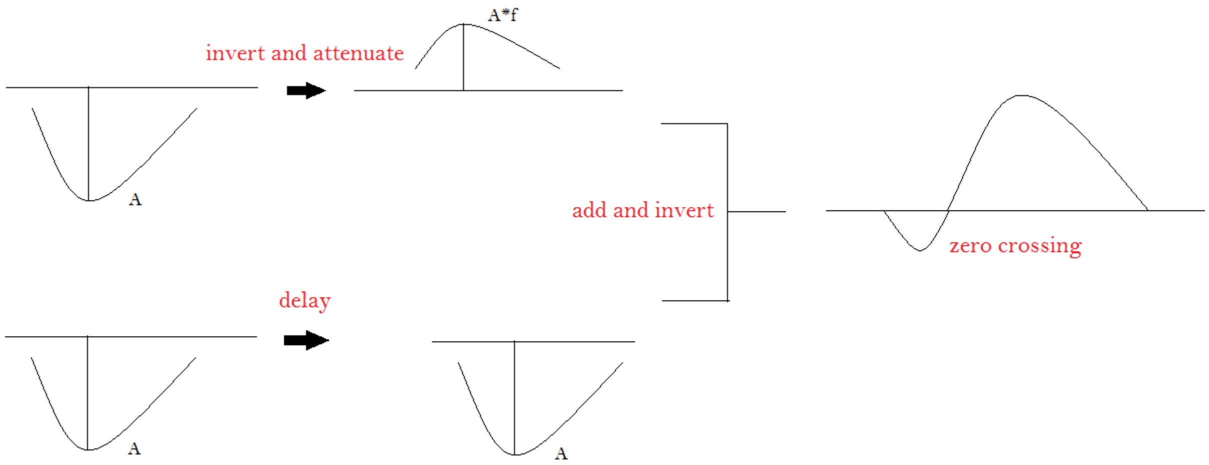


Figure 2.1: The flow diagram of the working of the circuit

2.1.1 Creating an inverted attenuated signal

Applying the golden rule at the V_- and V_+

$$\frac{V_{in}}{R_1} = -\frac{V_{out}}{R_2}$$

$$V_A = V_{out} = -\frac{R_2}{R_1} * V_{in}$$

Thus the fraction

$$f = \frac{R_2}{R_1}$$

$R_1 = 10k\Omega$ and $R_2 = 1k\Omega$

The other line of the signal is just made to pass through, assuming delay along the path to be less than the rise time, i.e. less than order of $1\mu s$ so the the ARC method works.

2.1.2 Adding the two analog signals

In the second opamp in the schematic the two signals are added and inverted.

$$-\frac{V_{out}}{R_5} = \frac{V_A}{R_3} + \frac{V_B}{R_4}$$

$$R_3 = R_4 = R_5 = 1k\Omega$$

$$V_{out} = -(V_A + V_B)$$

2.1.3 Comparator and Pulse generator

Now finally the signal is put into a comparator with threshold voltage 0 Volts, as the resulting signal that we get has to be triggered at the zero crossing.

As soon as there is a trigger the IC 555 timer generates a pulse of fixed period by the R and C components used in the timer. The timer is operating in a monostable state. Thus when the input goes below $V_{cc}/3$ there is a pulse. To keep the consistency the input to the timer is the inverted pulse from the comparator so that a positive pulse can be generated by the timer which helps the DAQ to start.

$$time = 1.1 * R * C \approx 1\mu s$$

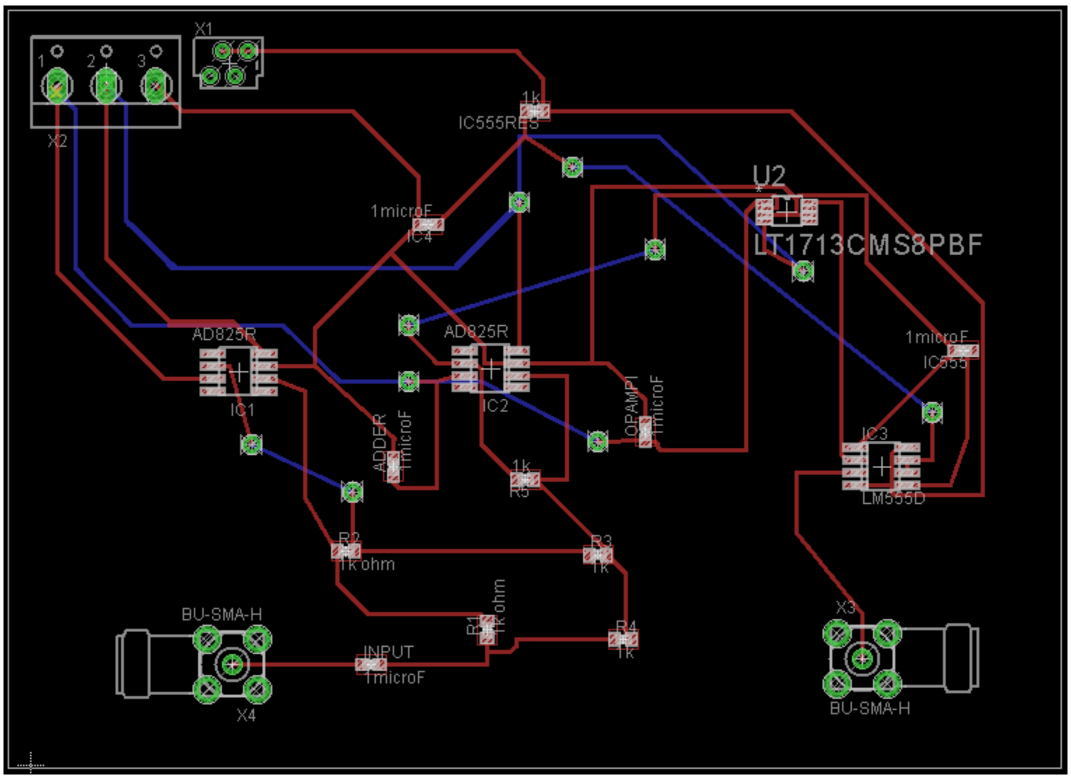


Figure 2.2: This is the **.brd** file in EAGLE.

2.2 Soldering

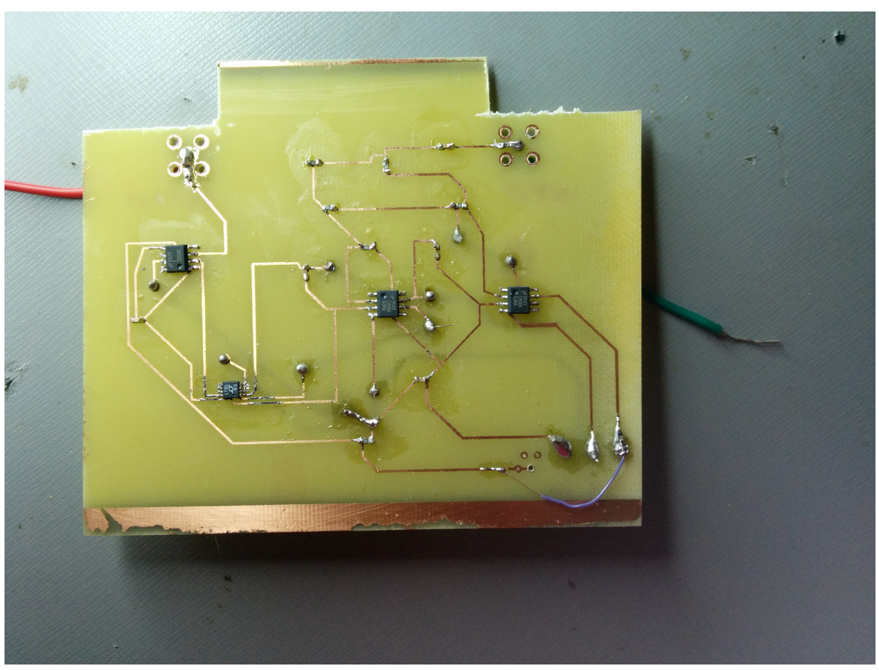


Figure 2.3: This is the soldered PCB from below.

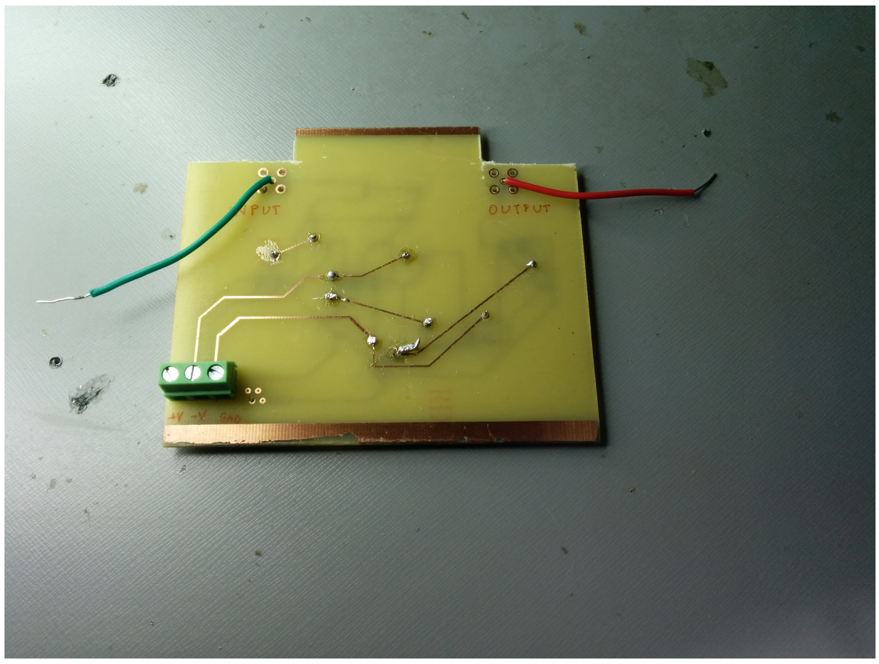


Figure 2.4: This is the top of the PCB.

2.3 Measurements

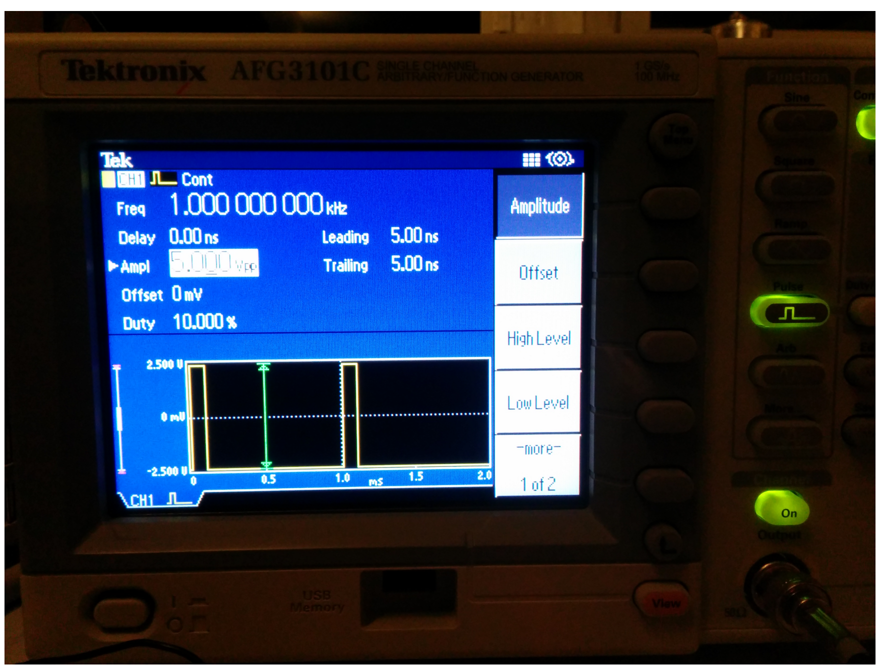


Figure 2.5: The test signal with a pulse of duty cycle 10% and 5 V_{pp} with frequency 1kHz

As can be seen, this was the test signal that was provided for the module.

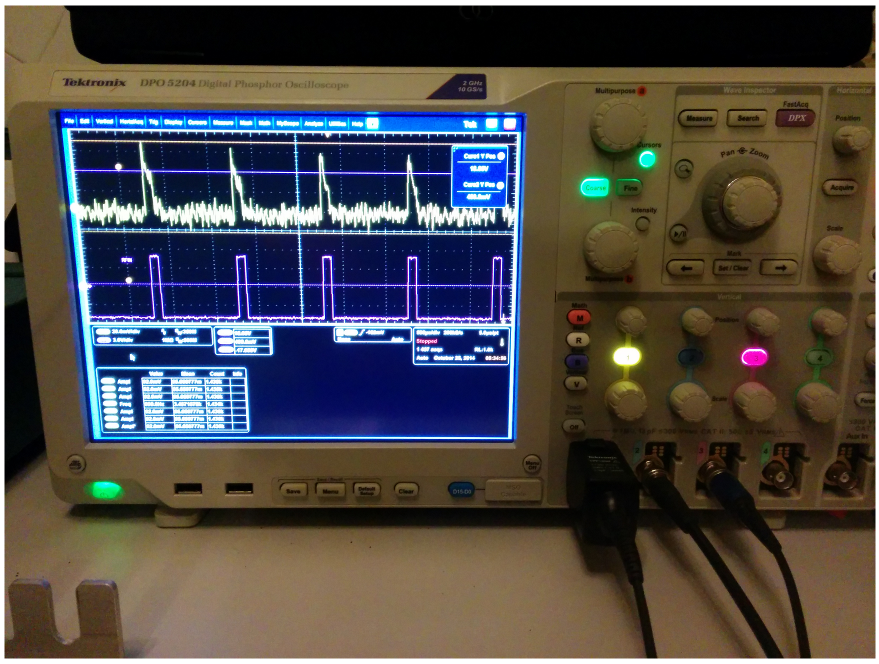


Figure 2.6: The reading on the oscilloscope

The purple signal is the input signal and the yellow signal is the output signal.

Conclusions and future work

The circuit is responding to the signal as expected but the signal to noise ratio is quite less. The possible reasons could be:
SMD soldering and circuit building by am an amateur might have affected. Probably the chemical etching PCB is not enough quality since it does not provide shielding. A further clever circuit design would probably decrease noise. Further more a rapid prototyped board needs to be fabricated for more robustness and stability of the circuit hardware. Expanding the horizon for circuit by making it work for any signal of any frequency, shape and characteristic.

References and Gratitude

- www.google.com
- www.wikipedia.com
- www.falstad.com/circuits/
- Techniques for Nuclear and Particle Physics Experiments by **William R. Leo** for a few figures and the methods.
- Software EAGLE.

I would like to thank **Prof. Pradeep Sarin** for giving me the opportunity to work under him and providing a really well equipped laboratory to me. I would like to thank **Aditi Udupa** for guiding me and **Varun Gandhi** to help me.

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